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1 **A 100 MHz 4 Mb cache DRAM with fast copy-back scheme**
Dosaka, K.; Konishi, Y.; Hayano, K.; Himukashi, K.; Yamazaki, A.; Hart, C.A.; Kumanoya, M.; Hamano, H.; Yoshihara, T.;
Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC, 1992 IEEE International , 19-21 Feb. 1992
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[Abstract]   [PDF Full-Text (260 KB)] **IEEE CNF**

2 **A 100-MHz 4-Mb cache DRAM with fast copy-back scheme**
Dosaka, K.; Konishi, Y.; Hayano, K.; Himukashi, K.; Yamazaki, A.; Iwamoto, H.; Kumanoya, M.; Hamano, H.; Yoshihara, T.;
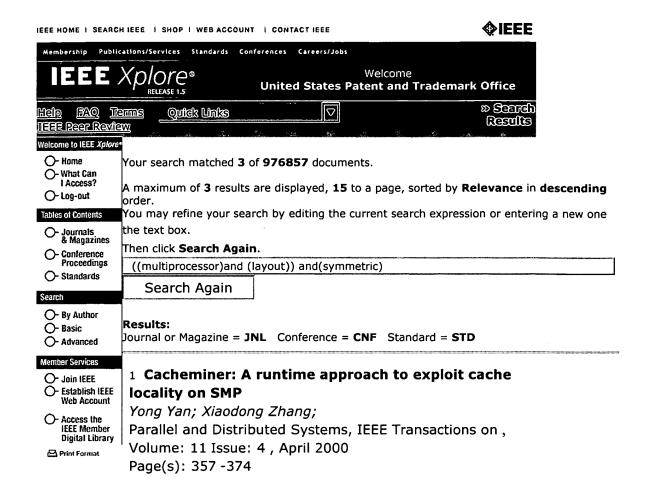Solid-State Circuits, IEEE Journal of , Volume: 27 Issue: 11 , Nov. 1992
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[Abstract]   [PDF Full-Text (608 KB)] **IEEE JNL**

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1 **Cacheminer: A runtime approach to exploit cache locality on SMP**
Yong Yan; Xiaodong Zhang;
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Volume: 11 Issue: 4 , April 2000
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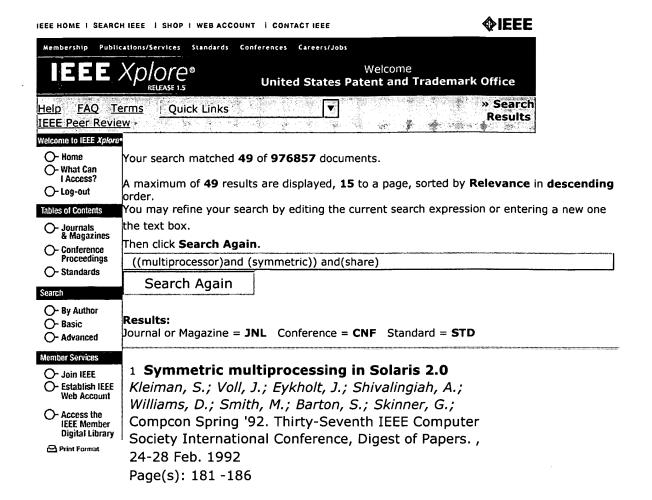
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